

Attorney's Docket No. 42P16806

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Shih-wei Liao et al.

Application No.: 10/676,889

Filed: September 30, 2003

For: METHODS AND APPARATUSES FOR  
COMPILER-CREATING HELPER  
THREADS FOR MULTI-THREADING

Examiner: Not Yet Assigned

Art Unit: Not Yet Assigned

Commissioner for Patents  
P.O. Box 1450  
Alexandria, Virginia 22313-1450

INFORMATION DISCLOSURE STATEMENT

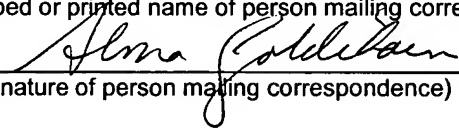
Sir:

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450 on December 16, 2003.  
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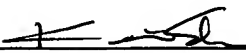
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If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 12/16, 2003

  
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U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. <sup>1</sup>	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> (Use as many sheets as necessary)		Application Number	10/676,889
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		Art Unit	Not Yet Assigned
		Examiner Name	Not Yet Assigned
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		42P16806	
<b>NON PATENT LITERATURE DOCUMENTS</b>			
Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T <sup>2</sup>
		CAROLE DULONG, et al., "An Overview of the Intel® IA-64 Compiler," Intel Technology Journal Q4 1999, 15 pages, Intel Corporation	
		GLENN HINTON, et al., "The Microarchitecture of the Pentium® 4 Processor," Intel Technology Journal Q1 2001, 13 pages, Intel Corporation. Downloaded from <a href="http://developer.intel.com/">http://developer.intel.com/</a> .	
		AMIR ROTH and GURINDAR S. SOHI, "Speculative Data-Driven Multithreading," appears in the Proceedings of the 7 <sup>th</sup> International Conference on High Performance Computer Architecture (HPCA-7), Jan. 22-24, 2001, 12 pages.	
		JERRY HUCK, et al., "Introducing The IA-64 Architecture," IEEE MICRO, September-October 2000, pages 12-23, IEEE, Los Alamitos, CA, USA.	
		DEBORAH T. MARR, et al., "Hyper-Threading Technology Architecture and Microarchitecture," Intel Technology Journal Q1 2002, 12 pages, Intel Corporation. Downloaded from <a href="http://developer.intel.com/">http://developer.intel.com/</a> .	
		STEVE S. W. LIAO, et al., "Post-Pass Binary Adaptation for Software-Based Speculative Precomputation," PLDI'02, June 17-19, 2002, Berlin, Germany, pages 117-128.	
		JAMISON D. COLLINS, et al., "Speculative Precomputation: Long-range Prefetching of Delinquent Loads," IEEE 2001, pages 14-25.	
		DONGKEUN KIM and DONALD YEUNG, "Design and Evaluation of Compiler Algorithms for Pre-Execution," ASPLOS X, 10/02, San Jose, CA, USA, pages 159-170.	
		ROBERT S. CHAPPELL, et al., "Simultaneous Subordinate Microthreading (SSMT)," IEEE, 1999, pages 186-195.	
		HIRALAL AGRAWAL and JOSEPH R. HORGAN, "Dynamic Program Slicing," Proceedings of the ACM SIGPLAN'90 Conference on Programming Language Design and Implementation, White Plains, New York, June 20-22, 1990, pages 246-256.	
		KARTHIK SUNDARAMOORTHY, et al., "Slipstream Processors: Improving Both Performance and Fault Tolerance," A.C.M. (ASPLOS), Cambridge, MA, USA, Nov. 12-15, 2000, pages 257-268.	

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		CRAIG ZILLES and GURINDAR SOHI, "Execution-based Prediction Using Speculative Slices," IEEE, 2001, pages 2-13.		
		JAMISON D. COLLINS, et al, "Dynamic Speculative Precomputation," IEEE 2001, pages 306-317.		
		ANDREAS MOSHOVOS, et al, "Slice-Processors: An Implementation of Operation-Based Prediction," ICS '01, Sorrento, Italy, ACM 2001, pages 321-334.		
		SHIH-WEI LAIO, et al, "SUIF Explorer: An Interactive and Interprocedural Parallelizer," PPOPP '99, 5/99, Atlanta, GA, USA. 1999 ACM, pages 37-48.		
		DEAN M. TULLSEN, et al., "Simultaneous Multithreading: Maximizing On-Chip Parallelism," ISCA '95, Santa Margherita, Ligure, Italy, 1995 ACM, pages 392-403.		
		CHI-KEUNG LUK, "Tolerating Memory Latency Through Software-Controlled Pre-Execution in Simultaneous Multithreading Processors," IEEE 2001, page 40-51.		
		RAKESH GHIYA, et al., "On the Importance of Points-To Analysis and Other Memory Disambiguation Methods for C Programs," PLDI 2001 6/01, Snowbird, Utah, USA, 2001 ACM ISBN, pages 47-58.		
		MURALI ANNAVARAM, et al., "Data Prefetching by Dependence Graph Precomputation," IEEE 2001, pages 52-61.		
		HONG WANG, et al., "Speculative Precomputation: Exploring the Use of Multithreading for Latency," Intel Technology Journal Q1 2002. Vol. 6 Issue 1, 14 pages, Intel Corporation. Downloaded from <a href="http://developer.intel.com/">http://developer.intel.com/</a> .		
		XINMIN TIAN, et al., "Intel® OpenMP C++/Fortran Compiler for Hyper-Threading Technology: Implementation and Performance," Intel Technology Journal Q1 2002. Vol. 6 Issue 1, 11 pages, Intel Corporation. Downloaded from <a href="http://developer.intel.com/">http://developer.intel.com/</a> .		

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